REMARKS

Claims 1-11 are pending in this application. By this Amendment, claims 1, 2 and 5 have been amended. The applicants respectfully submit that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated March 22, 2002.

IDS:

It is respectfully submitted that reference 64-2371 which is properly listed on the June 28, 2001 Information Disclosure Statement corresponds to reference 6-71011.

Title of the Invention:

The title of the invention has been objective to for being non-descriptive of the applicant's claimed invention. The applicant respectfully requests reconsideration of this objection.

As indicated above, the title of the invention has been amended, in its entirety, so as to read as follows:

> COMPOUND SEMICONDUCTOR DEVICE HAVING A MESFET THAT RAISES THE MAXIMUM MUTUAL CONDUCTANCE AND CHANGES THE MUTUAL CONDUCTANCE

It is believed that such amended title of the invention is now descriptive of the claimed invention.

In view of the above, the applicant respectfully requests that the title of the invention, as submitted herewith, be approved by the Examiner, and that the outstanding objection to the title be withdrawn.

Claims Objections:

Claims 1 and 5 stand object to in item 4 of the Action due to minor informalities. Claims 1 and 5 have been amended to correct such informalities. Accordingly, withdrawal of the rejectin is respectfully solicited.

35 U.S.C. §112, Second Paragraph, Rejection:

Claims 1-11 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

Claims 1 and 2 have been amended to overcome this rejection. Accordingly withdrawal of the rejection of claims 1-11 under 35 U.S.C. §112, second paragraph, is respectfully requested.

As To The Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1-5, 7, 8 and11 stand rejected under 35 U.S.C. §103(a) as being obvious over **Saito** (U.S. Patent No. 5,773,853) in view of Applicant's prior art Figs. 1 and 2;

2) claim 6 stands rejected under 35 U.S.C. §103(a) as being obvious over **Saito** in view of Applicant's prior art Figs. 1 and 2 and **Nakanishi** (U.S. Patent No. 5,477,066); and

3) claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being obvious over **Saito** in view of Applicant's prior art Figs. 1 and 2 in view of **Kuroda et al.** (U.S. Patent No. 5,837,565).

All of these rejections are respectfully traversed.

The invention in claim 1 relates to a compound semiconductor device, and is characterized to comprise a substrate formed of a first compound semiconductor, a graded channel layer formed on the substrate, and formed of a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by positioning a peak of a distribution of one constituent element into the inside and by continuously changing a ratio of the one constituent element in a thickness direction and doped with an impurity, a barrier layer formed on the graded channel layer, a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer, and a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer via the barrier layer.

The Examiner points out that **Saito** discloses a substrate (21) formed of a first compound semiconductor, a graded channel layer (23) formed on the substrate, similar to the grated channel layer in claim1, a burrier layer (24) formed on the graded channel layer, and a source electrode (S2), and a drain electrode (D2) formed both sides of the gate electrode (G2) to flow a current into the grated channel layer.

And, the Examiner points out **Saito** fails to disclose a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer, however Applicant's Prior Art Drawings disclose a semiconductor device where the gate electrode is formed on the barrier layer.

However, in col 7, lines 30 to 40 (Fig. 4B) of **Saito**, it is described that when $In_yGa_{1-y}As$ layer (23) and GaAs layer (24) is deposited with 20 cycles and a multi-layer made of GaAs/InGaAs layer (25) is formed, and "y" of $In_yGa_{1-y}As$ layer (23) becomes big as it becomes next deposition.

Accordingly, in **Saito**, a peak of distribution of In will exist in an end portion of a surface side of the GaAs/InGaAs layer (25) from above the description.

As opposed to **Saito**, in this application, it is made for an energy band gap to become the narrowest in inside of a layer in the graded channel layer by making the peak of the ratio of one constituent element exist in the inside (except both ends) of a layer.

In this matter, the peak of carrier density distribution is set to position into the inside not the surface of the channel layer. Therefore, even if the fluctuation of the gate voltage, the reduction of the gate voltage, etc. is caused, the steep increase/decrease of the carrier density in the channel layer is suppressed and also the mutual conductance that is higher and more stable than the prior art is obtained.

It is not described in **Saito** that the making the peak of the distribution of one constituent element exist in the inside (except both ends) of a layer so that an energy band gap becomes the narrower in the inside of a layer in the graded channel layer.

In view of the aforementioned remarks, claims 1, 2 and 5, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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Enclosures: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/893,477

IN THE CLAIMS:

Claims 1, 2 and 5 have been AMENDED to read as follows:

1. (AMENDED) A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a graded channel layer formed on the substrate, and formed of a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by [positioning] making a peak of [a] distribution of one constituent element exist [into] in the inside [and by continuously changing a ratio of the one constituent element] except the both ends in a thickness direction and [dosed] doped with an impurity;

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer.

2. (AMENDED) A compound semiconductor device according to claim 1, wherein the second compound semiconductor layer is composed of material that includes one constituent

element which is added in the first compound semiconductor, and the one constituent element has a function which makes the energy band gap of the second compound semiconductor layer narrower than that of the first compound semiconductor.

5. (AMENDED) A compound semiconductor device according to claim 4, wherein a peak of carrier density in the graded channel layer [sifts] shifts to the substrate side from a center of layer thickness of the graded channel layer.